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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,057	04/24/2006	Yohei Kanno	740756-2956	9926
22204	7590	09/16/2008	EXAMINER	
NIXON PEABODY, LLP			PHINAZEE, SIDNEY S	
401 9TH STREET, NW				
SUITE 900			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20004-2128			2815	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/577,057	KANNO ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	SIDNEY PHINAZEE	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 16 June 2008.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-6 and 13-18 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-6 and 13-18 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 4-24-06 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date <u>6-16-08</u> .	6) <input type="checkbox"/> Other: _____ .

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 1-3, 6, 13-15, and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al (6,448,578) in view of Murade (US 6,573,955 B2).

**Regarding claim 1**, Shimada discloses a semiconductor element comprising: a layer comprising titanium (3a) formed over a substrate (5); a gate electrode layer (3) formed over the layer; a gate insulating film (11) formed [[over]] in contact with the gate electrode layer; a semiconductor film (6) formed over the gate insulating film; a pair of n-type impurity regions (7, 8) formed over the semiconductor film; an insulating film (10) that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer (4, 9) formed over the pair of n-type impurity regions, But Shimada fails to teach wherein the layer comprising titanium is wider than the gate electrode layer. (Fig 1)

However Murade teaches wherein the layer comprising titanium (7) is wider than the gate electrode layer (2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a wider titanium layer than the gate electrode because the titanium layer would help with the heat dissipation of the device.

**As pertaining to claim 2,** Shimada discloses a semiconductor element comprising: a layer comprising titanium (3a) formed over a substrate (5); a gate electrode layer (3) formed over the layer; a gate insulating film (11) formed [[over]] in contact with the gate electrode layer; a semiconductor film (6) formed over the gate insulating film; a pair of n-type impurity regions (7, 8) formed over the semiconductor film; an insulating film (10) having a thickness of 100 nm or more (Column 6 lines 50-51) that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer (4, 9) formed over the pair of n-type impurity regions, But Shimada fails to teach wherein the layer comprising titanium is wider than the gate electrode layer. (Fig 1)

However Murade teaches wherein the layer comprising titanium (7) is wider than the gate electrode layer (2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a wider titanium layer than the gate electrode because the titanium layer would help with the heat dissipation of the device.

**As pertaining to claim 3,** Shimada discloses a semiconductor element comprising: a layer comprising titanium (3a) formed over a substrate (5); a gate electrode layer (3) formed over the layer; a gate insulating film (11) formed [[over]] in contact with the gate electrode layer; a semiconductor film (6) formed over the gate insulating film; a pair of n-type impurity regions (7, 8) formed over the semiconductor film; an insulating film (10) that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer (4, 9) formed over the pair of n-type impurity regions; wherein a thickness of a portion of the

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semiconductor film over which the insulating film is formed is thinner than that of the other semiconductor film, and the semiconductor film over which the insulating film (11) is formed has a thickness of 10 nm or more (column 6 lines 31-33), But Shimada fails to teach wherein the layer comprising titanium is wider than the gate electrode layer.

(Fig 1)

However Murade teaches wherein the layer comprising titanium (7) is wider than the gate electrode layer (2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a wider titanium layer than the gate electrode because the titanium layer would help with the heat dissipation of the device.

**Regarding claim 6,** Shimada in view of Murade teaches the limitations of claims 1-3 as discussed above. However Shimada discloses wherein the semiconductor element is incorporated in at least one selected from the group consisting of a TV reception set, an electronic book and a cellular phone (Columns 1 lines 11-17).

**Regarding claim 13,** Shimada discloses a semiconductor element comprising: a layer comprising titanium (3a) formed over a substrate (5); a gate electrode layer (3) formed over the layer; a gate insulating film (11) formed [[over]] in contact with the gate electrode layer; a semiconductor film (6) formed over the gate insulating film; a pair of n-type impurity regions (7, 8) formed over the semiconductor film; an insulating film (10) that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer (4, 9) formed over the pair of n-type impurity regions; and a pixel electrode (1) electrically connected to the conductive layer, But

Shimada fails to teach wherein the layer comprising titanium is wider than the gate electrode layer. (Fig 1)

However Murade teaches wherein the layer comprising titanium (7) is wider than the gate electrode layer (2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a wider titanium layer than the gate electrode because the titanium layer would help with the heat dissipation of the device.

**As pertaining to claim 14,** Shimada discloses a semiconductor element comprising: a layer comprising titanium (3a) formed over a substrate (5); a gate electrode layer (3) formed over the layer; a gate insulating film (11) formed [[over]] in contact with the gate electrode layer; a semiconductor film (6) formed over the gate insulating film; a pair of n-type impurity regions (7, 8) formed over the semiconductor film; an insulating film (10) having a thickness of 100 nm or more (Column 6 lines 50-51) that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer (4, 9) formed over the pair of n-type impurity regions; and a pixel electrode (1) electrically connected to the conductive layer, But Shimada fails to teach wherein the layer comprising titanium is wider than the gate electrode layer. (Fig 1)

However Murade teaches wherein the layer comprising titanium (7) is wider than the gate electrode layer (2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a wider titanium layer than the gate electrode because the titanium layer would help with the heat dissipation of the device.

**As pertaining to claim 15,** Shimada discloses a semiconductor element comprising: a layer comprising titanium (3a) formed over a substrate (5); a gate electrode layer (3) formed over the layer; a gate insulating film (11) formed [[over]] in contact with the gate electrode layer; a semiconductor film (6) formed over the gate insulating film; a pair of n-type impurity regions (7, 8) formed over the semiconductor film; an insulating film (10) that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer (4, 9) formed over the pair of n-type impurity regions; and pixel electrode (1) electrically connected to the conductive layer; wherein a thickness of a portion of the semiconductor film over which the insulating film is formed is thinner than that of the other semiconductor film, and the semiconductor film over which the insulating film (11) is formed has a thickness of 10 nm or more (column 6 lines 31-33), But Shimada fails to teach wherein the layer comprising titanium is wider than the gate electrode layer. (Fig 1)

However Murade teaches wherein the layer comprising titanium (7) is wider than the gate electrode layer (2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a wider titanium layer than the gate electrode because the titanium layer would help with the heat dissipation of the device.

**Regarding claim 18,** Shimada in view of Murade teaches the limitations of claims 13-15 as discussed above. However Shimada discloses wherein the semiconductor element is incorporated in at least one selected from the group consisting of a TV reception set, an electronic book and a cellular phone (Columns 1 lines 11-17).

**As regards to claims 2, 3, 14, and 15,** Shimada in view of Murade discloses the claimed invention except for the lower values of 100 nm and 10 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a specific range, since it has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum or workable ranges involves only routine skill in the art. [In re Aller, 105 USPQ 233]

**Claims 4 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada in view of Murade as applied to claims 1-3 and 13-15 above and in further view of Jung et al (2003/0107039).

**As pertains to claims 4 and 16** Shimada in view of Murade discloses the limitations of claims 1-3, and 13-15 as discussed above. Shimada in view of Murade fails to disclose the limitations of claims 4 and 16. However Jung discloses wherein the insulating film (72, in Jung) comprises at least one selected from the group consisting of polyimide, acrylic (paragraph 0049), and a material which has a skeleton formed by a bond of silicon and oxygen, and which includes at least hydrogen as a substituent, or at least one selected from the group consisting of fluoride, alkyl group, and aromatic hydrocarbon as a substituent. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the insulating material with at least one of the specified materials, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. [In re Leshin, 125 USPQ 416]

**Claims 5 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada in view of Murade as applied to claims 1-3 and 13-15 above and in further view of Sasaki et al (6,956,236).

**As pertains to claims 5 and 17** Shimada in view of Murade discloses the limitations of claims 1-3 and 13-15 as discussed above. Shimada in view of Murade fails to disclose the limitations of claims 5 and 17. However Sasaki discloses wherein the layer comprises titanium oxide (40b Fig 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the layer with the specified material, since it has been held to be with the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. [In re Leshin, 125 USPQ 416]

***Response to Arguments***

Applicant's arguments with respect to claims 1-6 and 13-18 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SIDNEY PHINAZEE whose telephone number is (571)270-5020. The examiner can normally be reached on Mon-Fri 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth A Parker/  
Supervisory Patent Examiner, Art Unit 2815

/SSP/